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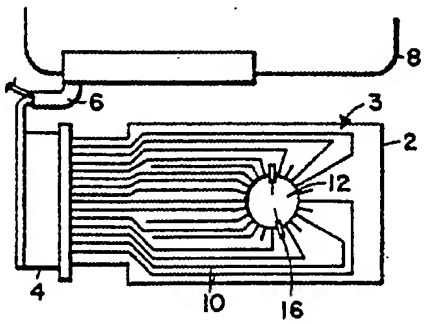
(54) Title: PROBE AND INTERFACE DEVICE FOR INTEGRATED CIRCUIT WAFERS

(57) Abstract

Probe device for testing integrated circuit wafers. The probe device comprises a support means (3), which has a plurality of metalized portions (10), and an aperture (12). A plurality of „L" shaped holding means (16), each having a thin metalized edge surface (18), are coupled to metalized portions of the support means so that a portion of the holding means extends into the aperture. The flat surface (28) of said holding means has conductor and resistant patterns (Figure 7) for the construction of active and passive hybrid circuitry to be used as buffers, terminations, loads and a general interface between the circuit under test and the circuit testing apparatus. A needle-like probe member (20) is coupled to a second metalized edge surface (30) of each of the holding means. These probe members are coupled to the holding means in such a manner that their curved portions extend into the support means aperture so as to electrically contact a circuit wafer placed therein, and electrically couple the circuit wafer to the support means and subsequently to the hybrid circuitry present on the support means. The hybrid circuitry may then be coupled to the support means and subsequently to the circuit testing apparatus via the first metalized edge surface as described above.



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PROBE AND INTERFACE DEVICE FOR INTEGRATED CIRCUIT WAFERS

Field of the Invention

The present invention relates to the field of integrated circuit testing device, and more specifically to probe type devices for testing integrated circuit wafers.

Prior Art

In the modern manufacture of integrated circuits, several hundred to several thousand integrated circuit chips are fabricated on a single wafer. In such a batch fabrication process, the yield of usable integrated circuits may be very low. Due to this low yield, a method has been developed to test each individual chip on the wafer to determine the functional integrated circuits contained therein. Without such a method, each integrated circuit chip must be severed from the wafer and mounted so that it may be tested individually.

Presently, probe cards are being utilized during the manufacture of integrated circuits to determine the usability of the individual circuits. In general, these probe cards consist of multi-probe members which are mechanically held in contact with the circuit wafers. Such mechanical contact allows electrical testing of the individual integrated circuits prior to their severance from the wafer. Thus, the required input voltages and input signals may be provided to the individual integrated circuit and the resulting output signals may be monitored. Often, it is desired to use these probe cards to couple high frequency signals to the integrated circuit wafers and to allow monitoring of high frequency output signals. Also, it would be valuable to use these probe cards at elevated temperatures to determine if the integrated circuits are functional at such temperatures.

One prior art attempt to provide the testing capabilities noted above is what is generally referred to as the blade probe card. The blade probe card consists of

an epoxy-glass printed circuit card to which is affixed a plurality of beryllium-copper blades. A metal needle-like probe is then soldered to each blade and all the probes are configured so that they may contact the pads of an integrated circuit chip on a wafer.

The blade probe card, however, has several distinct disadvantages. The greatest disadvantage is its high electrical capacitance between circuit paths resulting from the parallel configuration of the metal blades. That is, the necessary closeness and parallelism of the metal blades results in a capacitive effect between the individual blades. Due to this high capacitance, the blade probe card cannot be used for testing a variety of integrated circuits, including metal-oxide silicon (MOS) circuits, and for general high frequency testing.

A further disadvantage of the blade probe card results from the low surface resistance and low dielectric constant of the epoxy-glass material. Such probe cards optimally should have infinite surface resistance to allow total isolation of the circuit paths. However, since the epoxy-glass material has a low surface resistance, the individual circuit paths are allowed to interact to the detriment of integrated circuit testing. Also, the low dielectric constant of the epoxy-glass material limits the upper frequency at which the card can be used because of the resulting higher capacitance between individual circuit paths.

A second prior art attempt to provide the testing capabilities noted above is the epoxy-ring card. This card consists of an epoxy-glass card which has probes soldered to copper strips which are affixed to the epoxy-glass. However, the epoxy-ring card also has a variety of disadvantages. One disadvantage, difficulty of repair, stems from the method of affixing the copper strips to the epoxy-glass. The copper strip is laminated or glued to the epoxy-glass and the probe is then soldered to the strip. If a probe becomes damaged and must be

replaced, a new probe will have to be soldered to the copper strip. However, this heating of the strip causes the adhesive which holds it to the card to degrade, allowing the strip to move up and away from the card. Such damage to the copper strips prevents the card from being used again. Repaid of the epoxy-ring card is further hindered by the difficulty of properly aligning the new probe with the original probes.

Another problem associated with the epoxy-ring card is the flexibility of the card. Since such cards are not rigid, the individual probes soon lose their planarity and alignment with other probes. Such lack of planarity, as in the case of the blade probe card, results in damage to the circuit wafers and variation in contact resistance.

Further disadvantages of the epoxy-ring card, just as in the blade probe card, are a consequence of the utilization of epoxy-glass material. The epoxy-ring card also cannot be used at elevated temperatures since the plastic components of the glass material will deteriorate. In addition, the low surface resistance of the glass material and its low dielectric constant allows interaction of the input and monitoring lines as well as limiting its high frequency use.

Both of the probe card types described above have the common problem of probe to probe capacitance and line to line capacitance on the PC board which limits the use of the card for high frequency and/or high impedance and high gain test applications. A third type of card utilizing ceramic holders, to which individual needle-like probe members are attached, solves part of the problems inherent in the blade and epoxy-ring cards. The ceramic probe holders are inherently low capacitance and insensitive to high temperatures. They may be attached to a ceramic holder card which further decreases capacitance, temperature sensitivity and line to line leakages.

The major problem with all the presently available probe card techniques is the necessity to traverse a

significant distance through wire or printed circuit lines before test and measurement circuitry can be attached. This line length may present significant capacitance or inductive loading to high speed or high impedance circuitry. Present procedures involve building active buffer circuits and terminations on the probe cards, as close to the actual probe blades as possible, to provide line driving capability for connection to remotely located test equipment. With high speed, MOS or very high gain linear circuits, these techniques still leave much to be desired.

In many cases, the high speed circuitry cannot be tested at its full operating repetition rate and MOS circuitry is loaded excessively creating the necessity to test at a slower rate. Linear amplifiers may have to be tested at much less than full gain or with higher signal amplitudes than desired in order to compendate for probe capacitance and lead inductance. Noise pickup and generation is also increased by having measurement circuitry remote from the actual circuit connections.

Therefore, what is needed is a probe card which allows active circuits, buffers, loads and termination resistors effectively at the probe tip, thus eliminating the lead length between the needle-like probe contacting the integrated circuit under test and the measurement circuitry.

Summary of the Invention

Accordingly, it is an object of this invention to provide an improved probe testing device for testing electronic devices.

It is a further object of this invention to provide an improved probe testing card for testing either integrated circuit chips, hybrid circuits or discrete devices.

It is a still further object of this invention to provide an improved probe testing card having circuit means located adjacent to the probe tip for testing either integrated circuit chips, hybrid circuits or

discrete devices.

It is another object of this invention to provide an improved probe testing device which overcomes the above described problems associated with prior art probe testing devices.

Description of the Invention

The present invention is a probe device for testing integrated circuit wafers. The probe device comprises a support means, a plurality of holding means, hybrid circuitry constructed upon said holding means, and a plurality of corresponding needle-like probe members.

The support means is a rectangular or round structure having a generally circular aperture, and electrically conductive portions. Coupled to the support means in a plurality of "L" shaped holding means. These holding means have an extremely thin metalized area along their bottom edge surface which is used to connect them to the support means. A portion of the holding means extends into the circular aperture of the support means. Coupled to the holding means is a plurality of corresponding needle-like probe members, each having a curved portion. The narrow edge surface on the lower portion of the holding means also has an extremely thin metalized area. This metalized area is not connected to the other metalized area used for connection to the support means. Each probe member is coupled to this second metalized area so that the probe member is parallel to the support means while the curved portion of the probe member extends into the circular aperture. The furthest extreme of each probe member is configured so as to be capable of electrically contacting a circuit wafer which is placed within the aperture. Hybrid circuitry is constructed on the flat areas of the sides of the holding means. This hybrid circuitry is used to interface between the probe member and the connection to the support means and subsequently to the test and measurement circuitry. By this manner of electrical coupling, individual conductive portions of

the support means are electrically coupled to their corresponding holding means which are in turn electrically coupled to the hybrid circuitry on the holding means which is subsequently coupled to the corresponding probe member which is in turn electrically coupled to contact pads on the integrated circuit chip under test.

By utilization of the specific configuration more fully described below, the present invention allows testing of integrated circuit wafers at high frequency and under conditions which would not otherwise be possible. The ability to couple inputs and outputs from the integrated circuit wafer to hybrid circuit buffers, loads, drivers and termination devices in close proximity to the integrated circuit wafer, allows testing of the device which more closely approximates its final packaged form. The problem of outputs on the integrated circuit chip having to drive wire connections from the probe needles to the printed circuit lines on the holding means, subsequently driving long cables to the test equipment with associated problems of inductive and capacitive loading on the output, is virtually eliminated. The ability to place an equivalent load in immediate proximity to the integrated circuit output allows the measurement of propagation delays in a much more accurate manner without the problem of transmission lines delays which occur when the load is placed at a remote location from the integrated circuit. Correspondingly, when the driver for integrated circuit inputs is placed at a remote location, the problems are noise pickup on the input line as well as inherent delays. These are eliminated by the use of hybrid circuit drivers in close proximity to the integrated circuit input. Cross-coupling between lines connected to the integrated circuit pads is also greatly reduced by the reduction of lead length made possible by using the hybrid circuit technique on the probe holders. This technique reduces the free wire length emanating from each integrated circuit connection to the length required for a probe needle and a short connection to the hybrid circuit on the probe

holder. The signal can then be impedance converted to reduce the effect of cross-coupling on the support means and subsequently in the cable assembly leading to the test equipment. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objectives and advantages thereof, will be better understood from the following description considered in connection with the accompanying drawings in which a presently preferred embodiment of the invention is illustrated by way of example. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only, and are not intended as a definition of the limits of the invention.

Brief Description of the Drawings

Figure 1 is a top view of the probe device of the present invention and its corresponding testing apparatus;

Figure 2 is an enlarged top view similar to Figure 1 showing the probes, probe holders and support therefor for the portion of the probe device in proximity to the chip to be tested;

Figure 3 is a perspective view of the holding member used to hold the probe tip showing hybrid circuit connection paths and resistors;

Figure 4 is a view similar to Figure 3 with the attachment of a corresponding probe member;

Figure 5 is an electrical schematic diagram of the hybrid circuit buffer used in the probe device of Figure 1;

Figure 6 is a top view of the bonding pad configuration of the integrated circuit chip used in the hybrid circuit of Figure 5;

Figure 7 is an enlarged top view of the layout on a holding member substrate of the hybrid circuit of Figure 5 with the integrated chip of Figure 6; and

Figure 8 is a view similar to Figure 3 showing an alternate embodiment of the holding member.

Detailed Description of the Invention

Referring to Figure 1, probe device 2 is illustrated with its corresponding testing instrumentation 8. Testing instrumentation 8 is coupled to probe device 2 by means of cable 6 and coupling connector 4. Also illustrated in Figure 1 is support means 3 and its metalized portions 10. The metalized portions 10 may be implemented by silk screening onto ceramic, plastic or other suitable material or by etching and/or plating methods applied to standard printed circuit boards. If a silk screening process is used, the resulting assembly may be fired at high temperature causing the metalized portions to fuse directly to the support means 3, essentially becoming a part of it. By this method of application, the metalized portions 10 have little tendency to lift from support means 3 when heat is applied. This allows the metalized portions 10 to be repeatedly soldered during construction or repaid of probe device 2 without degradation. The use of silk screening techniques for implementing metalized portions 10 on the support means 3 is also compatible with the implementation of hybrid circuitry. Screening techniques may also be used to implement resistors on the support means 3. This permits portions of test related circuitry to be implemented directly on the support means 3, thus reducing size and physical distance from the integrated circuit under test and the measurement circuitry. Figure 1 also illustrates circular aperture 12 of support means 3. The particular integrated circuit to be tested on the integrated circuit wafer is located immediately beneath the circular aperture 12 and holding means 16.

Now referring to Figure 2, an enlarged view of the circular aperture 12, holding means 16 and probe member 20 can be seen. Probe members 20 are needle-like members which are made of tungsten or similar metal. Probe members 20 are coupled to holding means 16 in a manner which will be more fully described below. Probe tips 21 are aligned and configured such that they may make

electrical contact with metalized pads on the integrated circuit chip to be tested. In operation, the probe device 2 is placed in a rigid holder over an integrated circuit wafer located below the circular aperture 12. The wafer is aligned such that the metalized pads on the surface of a chip align with the array of probe tips 21. The wafer is normally held in place on a flat movable chuck by vacuum applied to the back of the wafer through holes in the chuck. In order to make mechanical and electrical contact between the probe tips 21 and the metalized pads on the integrated circuit chip, the chuck may be raised until the probe tips 21 contact the chip. In this manner, electrical connection is made from the integrated circuit pads through the probe member 20 to the metalized portion of the holding means 16 to which the probe member 20 is attached. This metalized portion is then directly connected to hybrid circuitry on the holding means 16. This configuration results in a very short physical connection between the integrated circuit pad and buffering or measurement circuitry which may be implemented on the holding means 16.

Figure 3 shows in greater detail the "L" shaped holding means 16 with its elongated portion 26 and its shortened portion 24. Along the bottom periphery of the elongated portion 26 of holding means 16 is a thin metalized portion 18. A second metalized portion 30 is applied to the bottom periphery of the shortened portion 24 of holding means 16. These metalized portions are applied to the narrow surface of the holding means 16 by silk screening and subsequent firing at high temperature. The first metalized portion 18 is used to make mechanical and electrical connection to support means 3. The second metalized portion 30 is used to attach the probe member 20 to the holding means 16. Additional metalized areas and resistor patterns are silk screened on the flat surface 28 of the holding means 16. Connection is also made between metalized conductors on the flat surface 28 and the

metalized areas 18 and 30 on the edge of holding means 16. This construction permits hybrid circuitry to be implemented on the holding means flat surface 28 and serves as an interface between electrical signals associated with the testing apparatus 8 (see Figure 1) and the integrated circuit chip under test.

Figure 4 shows in greater detail the preferred embodiment of the coupling of probe member 20 to the support means 16. Here, probe member 20 is soldered to metalized portion 30 along the narrow surface of shortened portion 28. Of course, probe members may also be coupled to holding means 16 by brazing or welding to the metalized portion 30. Probe member 20 is coupled to holding means 16 so that the curved portion 23 of probe member 20 extends beyond holding means 16.

Figure 5 shows in schematic form a buffer circuit typical of the type which might be used to improve the capability of an integrated circuit chip output to drive long interconnect lines. In the preferred embodiment of the present invention, the circuit will serve for illustration of the concept as an example of a buffer implemented with hybrid circuit techniques on the holding means 16 (see Figure 3). Its input is connected to the probe member 20 via metalization portion 30 and its output is connected to metalization portion 18 and subsequently to a wire or cable 6 (see Figure 1) leading to the electrical test equipment 8. The buffer circuit in Figure 5 may be implemented using a standard integrated circuit operational amplifier 74 with appropriate resistors and metal interconnects. The inverting input IN-78 and the output 86 of the operational amplifier are connected together to implement the unity gain configuration. The output OUT 54 from the circuit is taken from this point and will subsequently be connected to metalized portion 18 (see Figure 3) of holding means 16. The non-inverting input IN+80 is driven from a voltage divider circuit formed by resistors 106, 108, 110 and 116. The input signal IN 92 to this

resistive divider comes from the probe member 20. Resistor 110 is selected in the proper ratio to resistor 116 to provide the desired attenuation of the input signal. This allows input signal voltages at IN 92 of larger voltage magnitude than could be tolerated at the IN+80 input to the operational amplifier. Alternate scaling ratios may be implemented by selecting resistor 108 or 106 in parallel with resistor 110. This selection is easily accomplished by alternate wire bonding configurations at the time of manufacture. Resistors 40 and 42 are connected respectively to the input offset trimming pads N2 76 and N1 84. The other ends of resistors 40 and 42 are connected together and returned to the positive supply V+ 44. Adjustment of resistors 40 and 42 by standard hybrid manufacturing techniques such as scribing, sand blasting or laser trimming allows the input offset error of the integrated circuit operational amplifier 74 to be adjusted to a value low enough so as not to introduce significant error to the voltage transfer function of the circuit. Power requirements of the operational amplifier are supplied by the positive supply V+44 which is connected to pad 88 and the negative supply V-34 which is connected to pad 82.

Figure 6 shows the topological layout of connection or bonding pads on the surface of the integrated circuit operational amplifier 74 to be used for illustration. This physical layout of pads will affect the form or layout of the illustrated hybrid circuit. It should be realized, however, that the concept of the instant invention is applicable to virtually any circuit type and the specific operational amplifer 74 and circuit chosen are for illustration of the principles only.

Figure 7 is an enlarged view of the holding means 16 with its associated hybrid circuitry and probe member 20. The probe member 20 is attached to the metalized portion 30 as previously described which is subsequently connected to the input line IN 92. A drop of epoxy 32 is

used in construction to add strength and rigidity to the probe member 20. The positive supply V+ 44, the negative supply V- 34, and the ground lead 69 are connected from the holding means to the support means by way of wires 72, 70 and 71, consecutively.

The integrated circuit operational amplifier is mounted on a large metalized pad area 55 which is connected to the negative supply lead 34. The V- pad 82 from the chip is connected to this supply lead 34 via wire bond 56. The positive supply is routed to the vicinity of the integrated cricuit chip via metalized trace 44. Wire bond 46 connects the V+ pad 88 to the positive supply lead 44. The monolithic ceramic capacitor 64 is used to bypass electrical noise between the positive supply lead 44 and the negative supply lead 34. The chip capacitor is attached by solder connections 66 and 68. The output pad OUT 86 from the operational amplifier is connected by wire bond 48 to the output metalized trace 54 and subsequently to metalized portion 18. Metalized trace 54 also connects to input lead IN 78 via wire bond 60. The input attenuator resistors 106, 108, 110 and 116 are formed by silk screening a resistive material directly onto the holding means and subsequently firing at a high temperature. The input lead IN 92 is connected to resistor 110. The other end of resistor 110 is connected to metalized trace 94 which is subsequently connected by wire bond 58 to the non-inverting input IN+ 80 of the operational amplifier. If wire bonds 98, 102, 104 and 112 are deleted, the circuit functions as a simple voltage follower with a resistor 110 in series with its input. The input resistance may be eliminated by making the connection from IN 92 to the trace 94 with wire bond 104. Maximum input attenuation would be achieved by connecting wire bond 112 from metalized trace 94 to metalized trace 114 thereby connecting resistor 116 into the circuit. In this configuration resistor 110 and resistor 116 form a voltage divider circuit thus reducing the potential present on input trace 92 to a predictable lower

level on trace 94 which is subsequently presented to the operational amplifier IN+ 80. Other division ratios are possible by proper selection of bonding wires 98 and 102. This technique allows the overall gain of the circuitry to be programmed at time of manufacture. Trimming resistors 40 and 42 are connected from the positive supply lead 44 to metalized traces 38 and 50, respectively. Metalized trace 38 is connected by wire bond 36 to pad N2 76 on the operational amplifier. Metalized trace 50 is connected by wire bond 52 to pad N1 84 on the operational amplifier chip. The circuit shown in the present example uses only a portion of the area available in the shortened portion 24 and the elongated portion 26 of the holding means. Essentially the entire area of the holding means 16 is available for construction of hybrid circuitry. The only restriction is that a small area must be maintained clear along the top of the holding means 16 in order to hold the device while attaching it to the support means.

Figure 8 shows an alternative to the preferred embodiment of the holding means. In order to eliminate the necessity of connecting wires to the holding means and subsequently to the support means, metalized portion 18 is made smaller and metalized portions 19, 21 and 23 are added to the bottom periphery of the elongated portions 26 of the holding means 16. Using the previously discussed buffer circuit as an example, the positive supply lead 44, negative supply lead 34 and the ground lead 69 are routed to the metalized portions 21, 34 and 69, respectively. The remainder of the hybrid circuitry on the holding means 16 would remain essentially unchanged. Metalized portion 30 still connects to metal trace 92 on the shortened portion 24 and metalized portion 18 still connects to metal trace 54 on the elongated portion 26 of holding means 16.

It can be seen from Figures 2 and 4 that there is little parallel surface area of electrical conductors along holding means 16. In particular the conductor area associated with the input circuitry IN 92 (see Figure 7) is

quite small. Because the capacitive coupling between adjacent holding means is a function of the adjacent parallel surface area, such a configuration greatly minimizes the capacitive effect between adjacent holding means 16. The capacitive loading on an integrated circuit output under test with this configuration is greatly reduced over the prior art method which coupled the integrated circuit output through the support means to a cable connected to the test equipment. The shortest practical length of cable between the electrical testing equipment and the connector to the support means would have many hundreds of times more capacitance than the input circuitry provided by the hybrid circuit on the support means. If the buffering circuitry were built on the support means rather than the holding means, the situation would be improved over having the integrated circuit output drive the cable, however, the capacitance loading presented by this arrangement would still be many times greater than is possible when the buffering circuitry is built directly on the holding means 16. In addition the inductive effects of the signal path from the probe member 20 to the support means and subsequently to the testing equipment are greatly reduced. Many high gain linear circuits and high speed digital circuits are intolerant of inductance in their input, output or supply leads. This can lead to oscillations in the high gain circuitry and oscillations or incorrect measurements in the high speed circuitry. Reducing the capacitive and inductive loading on the circuit outputs by use of the instant invention allows faster and more reliable testing to be accomplished.

Although the instant invention has been illustrated by discussion of a buffer circuit designed to reduce capacitive, inductive and resistive loading on an integrated cirucit output under test, it can be seen by one skilled in the art that virtually any type hybrid configuration would be possible on the holding means 16. Signal processing and filtering circuitry, sample and hold, input

wave shaping, waveform generation, comparator, voltage regulation, and digital storage circuitry are only a few of the many types of hybrid circuit configurations which might be implemented on the holding means 16. These circuits enable the user to interface effectively between the integrated circuit chip under test and the external test equipment without subjecting the unit under test to an unnatural condition such as a long cable or high capacitive or inductive loading. The concept may be extended to include hybrid circuitry constructed on the support means as well as on the holding means. Circuitry on the support means or on the holding means might be single or double sided in construction and could easily include lines of controlled impedance such as 50 or 75 ohm lines required for testing some high speed logic families. The use of metal covered with an insulating medium for the support means allows controlled impedance lines to be constructed on both sides of the support means. The use of metal also lends support and rigidity to the support means for better performance. Metal substrates also provide superior thermal conduction properties. A support means or a holding means constructed on insulated metal has the ability to dissipate heat very effectively from hybrid circuitry constructed upon it.

While the invention has been particularly shown and described in reference to the preferred embodiment thereof, it will be understood by those skilled in the art that suitable modification may be made therein without departing from the spirit and scope of the invention.

CLAIMS

1. A probe device comprising, in combination, a plurality of probe elements, and means for holding each of said probe elements, said means for holding each of said probe elements also comprising test circuit means electrically connected to each of said probe elements for permitting each of said probe elements to electrically test an electronic device.

2. A probe device in accordance with claim 1 wherein said means for holding each of said probe elements being located at the end of each of said probe elements opposite the portion of each of said probe elements used for contacting an electronic device.

3. A probe device in accordance with claim 1 including support means for supporting said holding means in a configuration to permit each of said probe elements to contact the electronic device under test.

4. A probe device in accordance with claim 3 wherein said means for holding each of said probe elements being located at the end of each of said probe elements opposite the portion of each of said probe elements used for contacting an electronic device.

5. A probe device in accordance with claim 3 wherein said support means comprising a printed circuit card.

6. A probe device in accordance with claim 5 wherein said printed circuit card having an insulating substrate and a plurality of metal conductors located on at least one surface of said insulating substrate.

7. A probe device in accordance with claim 6 wherein said insulating substrate comprising a ceramic substrate.

8. A probe device in accordance with claim 6 wherein said insulating substrate comprising an epoxy-glass substrate.

9 A probe device in accordance with claim 5

wherein said printed circuit card having a metal substrate, at least one insulating layer located on at least one surface of said metal substrate, and a plurality of metal conductors located on said one insulating layer.

10. A probe device in accordance with claim 5 wherein said printed circuit card having an aperture, said holding means being located around said aperture.

11. A probe device in accordance with claim 1 wherein said test circuit means comprising a printed circuit card.

12. A probe device in accordance with claim 11 wherein said printed circuit card having an insulating substrate and a plurality of metal conductors located on at least a surface of said insulating substrate.

13. A probe device in accordance with claim 12 wherein said insulating substrate comprising a ceramic substrate.

14. A probe device in accordance with claim 12 wherein said insulating substrate comprising an epoxy-glass substrate.

15. A probe device in accordance with claim 11 wherein said printed circuit card having a metal substrate, at least one insulating layer located on at least one surface of said metal substrate, and a plurality of metal conductors located on said one insulating layer.

16. A probe device in accordance with claim 11 wherein one end of each of said probe elements being connected to a separate one of said printed circuit cards.

17. A probe device in accordance with claim 3 wherein said test circuit means comprising a printed circuit card, said support means comprising a printed circuit card, means for electrically connecting conductors on said printed circuit card of said test circuit means of said holding means to said conductors on said printed circuit card of said support means.

18. A probe device in accordance with claim 17 wherein said means for electrically connecting conductors

comprising metalized edge portions on said printed circuit card of said test circuit means and said printed circuit card of said support means.

19. A probe device in accordance with claim 5 wherein said printed circuit card of said support means having at least one active and passive electrical devices connected to said printed circuit card.

20. A probe device in accordance with claim 11 wherein said printed circuit card of said test circuit means of said holding means having at least one of active and psssive devices connected to said printed circuit card.

21. A probe device in accordance with claim 17 wherein said printed circuit card of said support means having at least one active and passive electrical devices connected to said printed circuit card, said printed circuit card of said test circuit means of said holding means having at least one of active and passive devices connected to said printed circuit card.

22. A probe device in accordance with claim 20 wherein said test circuit means having a hybrid circuit located thereon.

23. A probe device in accordance with claim 21 wherein said printed circuit card of said support means having a hybrid circuit located thereon.

24. A probe device in accordance with claim 4 said support means comprising a printed circuit card, said printed circuit card having an insulating substrate and a plurality of metal conductors located on at least a surface of said insulating substrate, said insulating substrate comprising a ceramic substrate, said printed circuit card having an aperture, said holding means being located around said aperture, said test circuit means comprising a printed circuit card, said printed circuit card of said test circuit means having an insulating substrate and a plurality of metal conductors located on at least a surface of said insulating substrate, said

insulating substrate of said printed circuit card of said test circuit means comprising a ceramic substrate, one end of each of said probe elements being connected to a separate one of said printed circuit cards of said test circuit means of said holding means, including means for electrically connecting conductors on said printed circuit card of said test circuit means of said holding means to said conductors on said printed circuit card of said support means, said means for electrically connecting conductors comprising metalized edge portions on said printed circuit card of said test circuit means and said printed circuit card of said support means, said printed circuit card of said support means having at least one of active and passive electrical devices connected to said printed circuit card, said printed circuit card of said test circuit means of said holding means having at least one of active and passive devices connected to said printed circuit card.

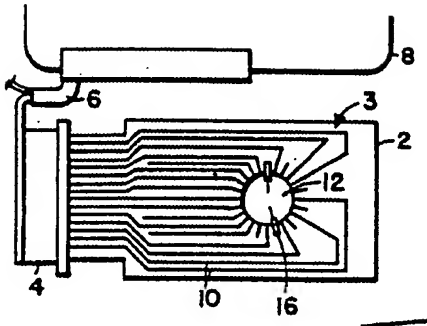


FIG. 1

FIG. 2

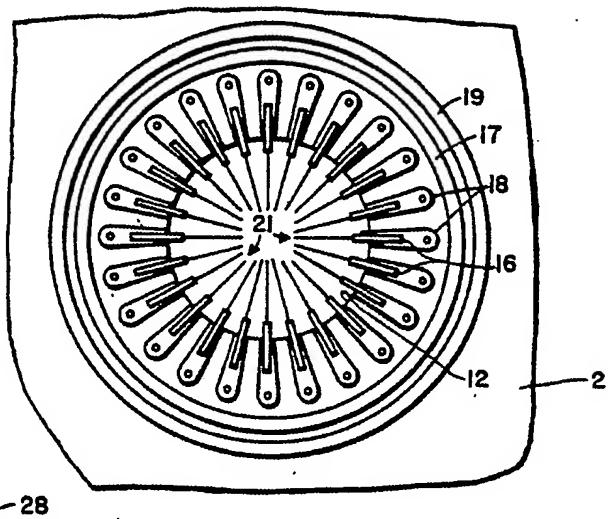
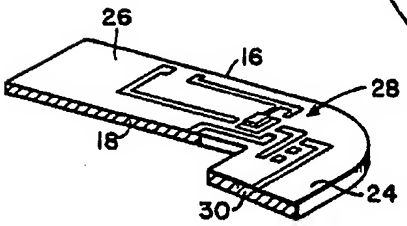


FIG. 3



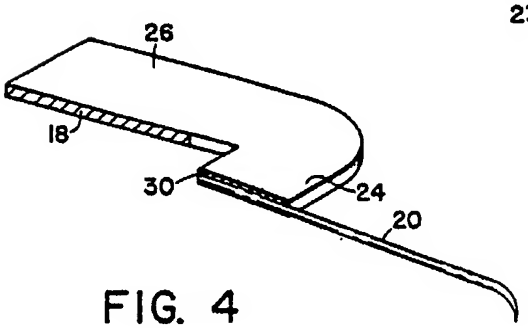


FIG. 4

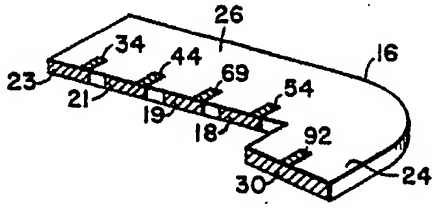


FIG. 8

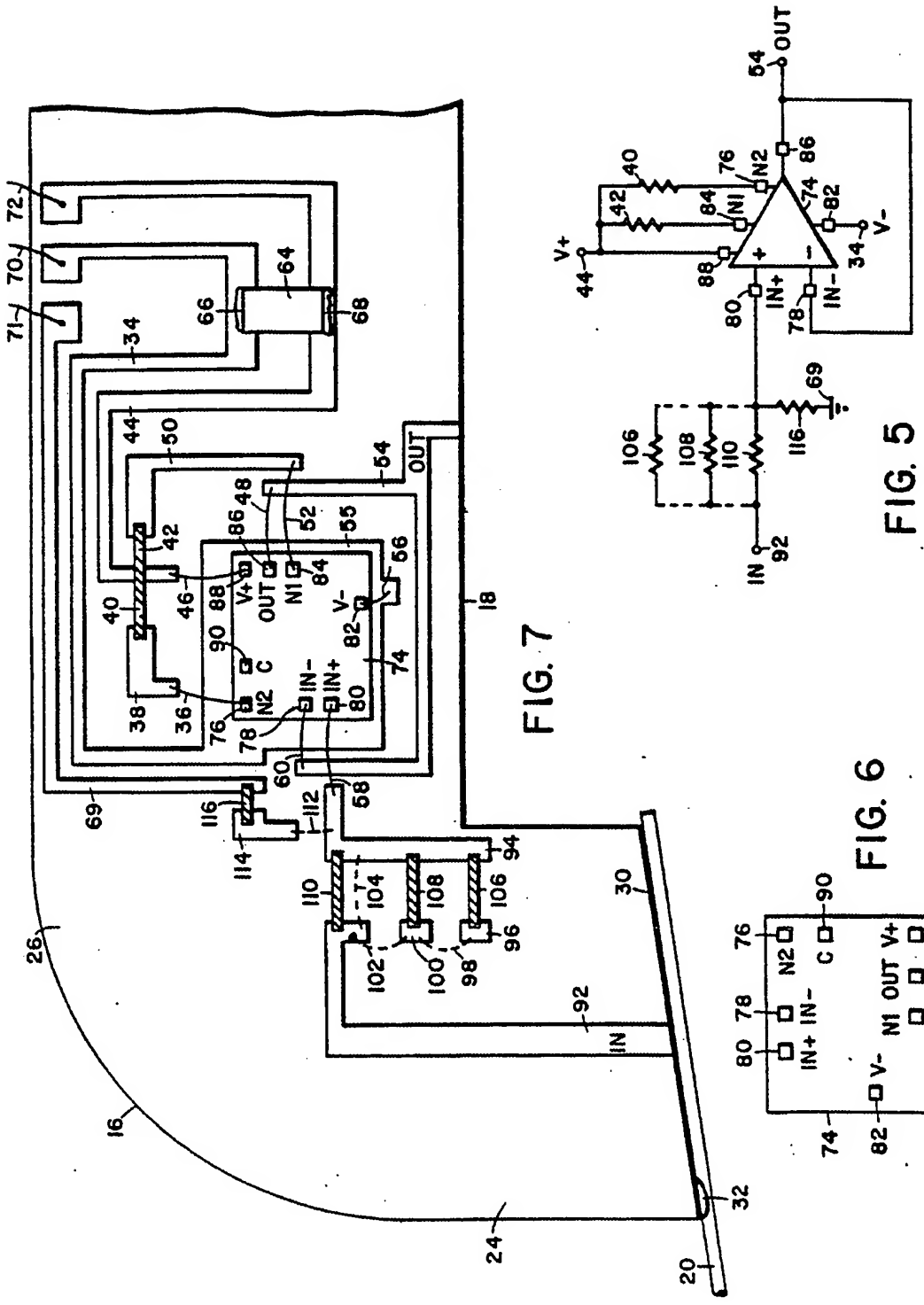


FIG. 5

FIG. 6

FIG. 7

INTERNATIONAL SEARCH REPORT WO 80/00101

International Application No PCT/US79/00444

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT CL. G01R 1/06; G01R 31/02
US CL. 324/158P, 158F, 72.5

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	324/158P, 158F, 72.5, 149 339/108TP

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
E	US, A, 4,161,692 Published 17 JULY 1979 TARZWELL	1-24
P	US, A, 4,116,523 Published 26 SEPTEMBER 1978 COBERLY ET AL	1-24

* Special categories of cited documents: [15]

"A" document defining the general state of the art
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"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention
"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
29 OCTOBER 1979	09 NOV 1979
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	Ernest F. Karlsen E. Karlsen

Form PCT/ISA/210 (second sheet) (October 1977)